IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Kelvin MA *et al.*	Docket No.:	6198.8-1
Serial No.:	10/648,717	Examiner:	Kianni, Kaveh C.
Filing Date:	August 26, 2003	Art Unit:	2883
Entitled:	Optical Interconnect And Method For Making The Same		

DECLARATION OF TODD R. TOLLIVER UNDER 37 C.F.R. SECTION 1.131

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I, Todd R. Tolliver, a co-inventor of the above-referenced patent application, enclose hereto as Exhibit A a true copy of an invention disclosure form, with dates and portions redacted as noted, which was received by the General Electric Patent and Legal Operation department of General Electric Company on a date prior to August 19, 2002, in the ordinary course of business as part of General Electric Company's invention disclosure program. In accordance with General Electric Company's invention disclosure program at that time, upon receipt of an invention disclosure document from an inventor, the invention disclosure document is assigned a docket number and a docket date by the Patent and Legal Operation department of General Electric Company.

CERTIFICATE OF MAILING/TRANSMISSION (37 C.F.R. §1.8(A))

MAILING

☒ I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:

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FACSIMILE

☐ I hereby certify that this paper is being transmitted to the Patent and Trademark Office facsimile number (703) 872-9306 on:

Date: July 11, 2005

Signature: Cindy C. Dioso

Cindy C. Dioso

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE

Todd R. Tolliver

Signature _____ Date: 7/7/05

Citizenship: United States of America

Residence: Clifton Park, New York

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GE Patent Disclosure Letter System

DOCKET NUMBER

30934

DOCKET DATE

Redacted

TITLE OF INVENTION

Multi-layer optical interconnection for optical integrated circuits

GE TECHNOLOGY AREA(S)

Redacted

PROJECT NAME

Redacted

PROJECT NUMBER

Redacted

PROJECT LEADER

Mahony, Michael

BUSINESS OR ORG. CONTACT INFORMATION

NAME John Soderberg

PHONE NUMBER Redacted

Was this invention first conceived or reduced to practice in the performance of work under a contract between GE and another non-government third party? Redacted

THIRD PARTY NAME Lockheed Martin

PHONE NUMBER Redacted

Date Invention Conceived : Redacted

Circumstances Invention Conceived i.e., described in patent notebook (include page #), technical report, letter, discussed in meeting minutes, etc.
Need to develop concept for optical integrated circuit for Lockheed Martin shared vision program

Was this invention first conceived or reduced to practice in the performance of work under a US Government contract?
Redacted

ABSTRACT OF THE INVENTION

Please write a brief explanation of the invention (Limit to 350 words)
A multilayer optical interconnection technology to allow high density integration of optical, electrical and opto-electronic components. Optical connections will be coupled through optical vias between different layers. Active optical components and devices are directly coupled horizontally with the optical waveguides on both side of the surfaces.

BACKGROUND OF THE INVENTION

Please describe the problem or requirement addressed by your invention.
The ever increasing clock speed of electronic circuits requires high-speed interconnects in order for these technologies to reach their full potential. However, electronic-based interconnection speed is limited and has become a bottelneck for information transfer on the printed circuit board. An optical-based interconnection system is highly desirable for enabling these high speed circuits to communicate with a minimum of delay. Although optical interconnects hold great promise, their implementation has proven quite difficult, especially for vertical connection through multiple optical interconnect layers, due to the differences in materials involved. Therefore, opto-electronic integrated circuits are labor and process intensive, which results in high manufacturing costs at low volumes. Most of the current optical waveguides for interconnecting optical components are restricted to a single layer.

How has this problem or requirement been addressed before?

There are many optical interconnect waveguides technologies developed. These technologies limits the optical

interconnection to a single layer due to the difficulty in connecting optical signals from different layer of interconnect at different level. Others tried to form a 45 degree angle at the end of the waveguides to deflect the light signal vertically to another layer of optical waveguides. But making the 45 degree angle on mulitple layers prove to be a difficult process.

Is this disclosure letter related to any GE disclosure letters, patent applications or issued patents?

Redacted

Have you completed a prior art search? Redacted

Please list any relevant literature or patents of which you are aware.

DETAILED DESCRIPTION OF THE INVENTION

How does your invention work?

There are two versions of the optical integrated circuit interconnection process. The first version is a single-sided process that results in active devices on only the top surface. The double-sided version describes a process to allow placement of active devices on the top and bottom of the structure. Please see attachment "how it works.txt" for full description.

Describe the important features of your invention and explain how to use the invention to solve the problems described above.

The invention enables integration of optical, electrical and opto-electronic components in a single heterogenous package. It uses established processing techniques to produce optical waveguides and optical vias which allow three-dimensional optical integration. The construction of the optical via is a simpler planar process unlike the 45 degree angled waveguides thus enabling multi-layer optical interconnections.

What advantages are provided by your invention?

The invention enables high-speed optical communication between components horizontally, as well as vertically. The simpler optical via construction which uses only conventional planar lithography buildup process as compared to the 45 degree angled waveguides enables easy multi-layer optical interconnections fabrication. These optical vias can also be used for complex wavelength management of the signals. This invention provides a technique for integrating optical, electrical and opto-electronic components in a single system.

Has your invention been reduced to practice? NO

Briefly describe any efforts to make a prototype of your invention or to test your invention. Additionally, summarize the results of any related experiments and testing and highlight any results of particular significance.
A computer simulated model was done to show the optical via (resonator) can be used to couple light signal from one waveguide onto another waveguide at different levels efficiently.

BRIEF DESCRIPTION OF THE DRAWINGS
Please describe the significance of any pictures, drawings, graphs, diagrams, structures or figures and the type of picture along with the specific view or application to the invention.
The first figure is a notional depiction of the overall assembly. The second and third figures are a pictorial description of the single-sided process. The fourth figure depicts the ability of the ring resonator optical via to direct light in the desired direction. The fifth, sixth and seventh figures give an overview of the double-sided process.

CLAIMED INVENTION
Please identify novel aspects that should be protected within this disclosure letter.
We claim the overall buildup process of the single-sided integrated assembly and double-sided integrated assembly structure. We also claim the optical resonator structure used between waveguides at different layers for coupling optical signals in a multi-layered optical interconnection.

ATTACHED FILES
OpticalICInterconnectProcess.ppt
how it works.doc

DUTY OF DISCLOSURE		
a.	**Have steps been taken to put into use, either outside GE or in our own operations?**	Redacted
b.	**Has the invention or a product embodying or using it been sold or offered for sale?**	Redacted
c.	**If the invention pertains to a process, have any steps been taken to employ the process commercially (e.g., for product production)?**	Redacted
d.	**Has the invention been described in an electronic or printed publication?**	Redacted

e.	**Has the invention been described to persons who are not employees of GE?**	Redacted
f.	**Are there results available of a prior art search pertaining to this invention?**	Redacted
g.	**Has anyone else associated with the project within GE (marketing, sales, sourcing, etc.) disclosed the invention or offered the invention for sale?**	Redacted
h.	**If you answered Questions a-g as "NO", is any use, sale, publication, or disclosure of the invention now contemplated?**	Redacted

Described to others who are NOT employees of GE?

To Whom? names/affiliations (company, university, etc.)

John Soderberg

By Whom?

Kelvin Ma

Where? (include Country)

Redacted

When?

Redacted

Is there an Nondisclosure Agreement(NDA) in place?

Redacted

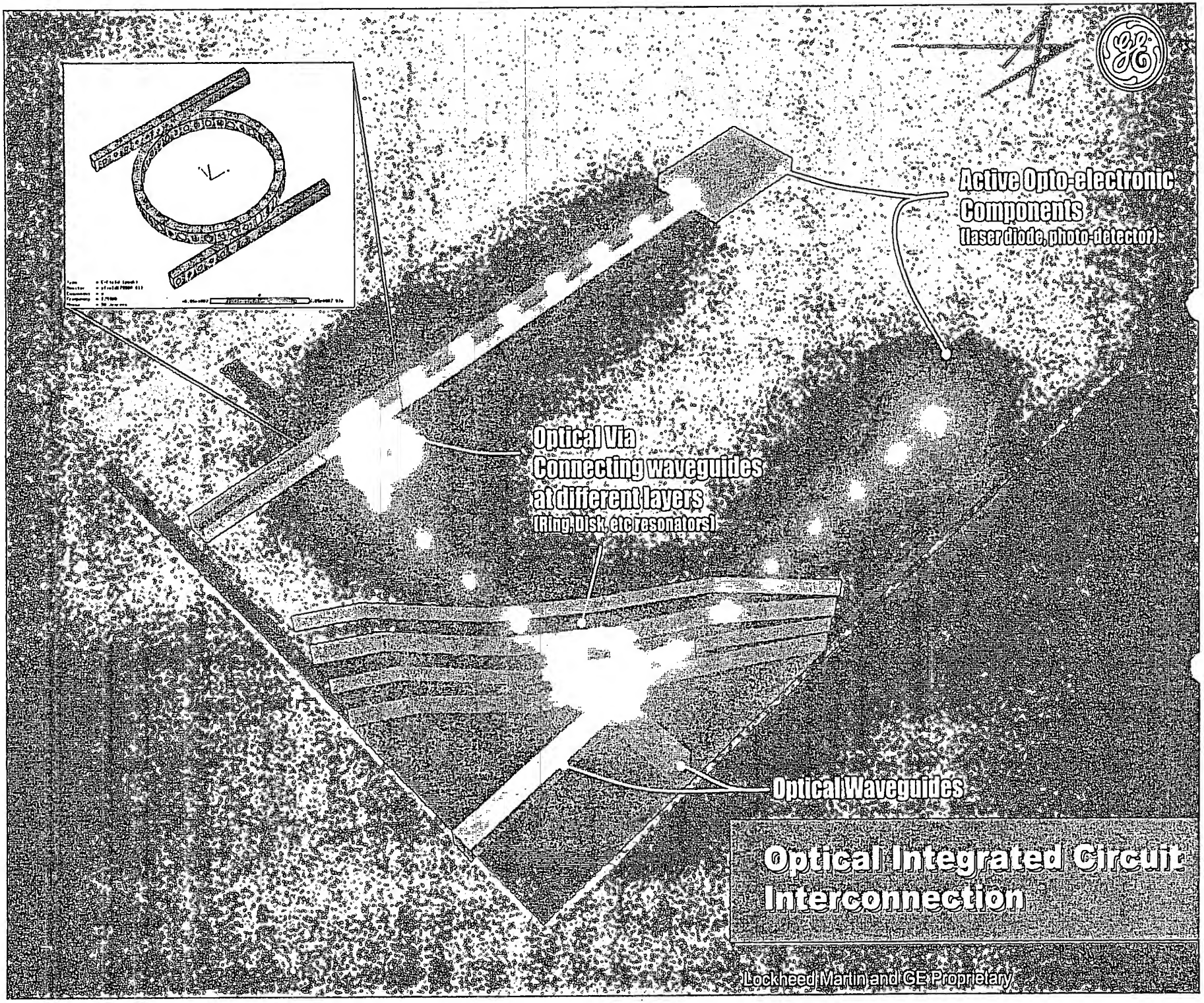
CO-INVENTORS			
Name	Address	Global Tech. Center	L
*Kelvin Ma	Redacted	Redacted	E
Todd Tolliver	Redacted	Redacted	A

**Lead co-inventor*

NON-GE CO-INVENTORS				
Name	Email	Citizenship	Company/University	Assign Rights to GE
John Soderberg	Redacted	Redacted	Lockheed Martin	

Associated Lab/Program: Redacted

Assigned Attorney: Redacted


Active Opto-electronic Components
(laser diode, photo-detector)
Optical Via
Connecting waveguides at different layers
(Ring, Disk, etc resonators)
Optical Waveguides
Optical Integrated Circuit Interconnection
Lockheed Martin and GE Proprietary

Optical Integrated Circuit Interconnection Process (1/2)

Single sided Optical Interconnect Circuit

1 Masking dopant region

Substrate (Si, GaAs, Sapphire, GaN, etc)

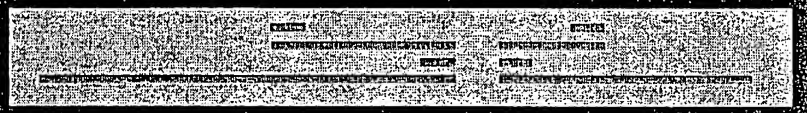
2 Creating dopant region for waveguides (ex: ion implantation)

3 Remove mask and continue growth process

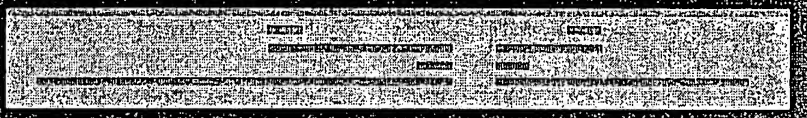
4 Creating dopant region for resonator (optical via)

5 Continue growth process and creating dopant region for next level of waveguides

6 Repeat step 1 to 4 for building additional intermediate optical interconnect layers



7 Blanket dope the entire top surface region



8 Mask optical waveguide region

9 Etch waveguide structures and chip pockets (ex: RIE)

10 Remove mask

Optical Integrated Circuit Interconnection Process (2/2)

Coat thin lower dielectric cladding layer (ex: sputtering)

11

Metalize reflective and conductor layer (ex: sputtering)

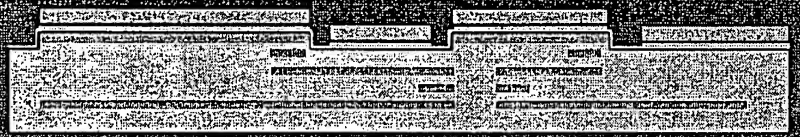
12

Mask out waveguide and electrical regions

13

Etch out metal

14



Remove Mask

15

Place down optical, optoelectronic and electronic components

16

Wire-bond components onto metal contacts and connections

17

Optional final encapsulation of module

18

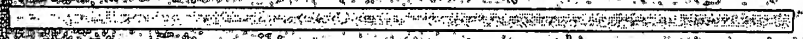
- **Highly integrated optical, electrical and opto-electonic module.**
- **Fully compatible with existing semiconductor processes**
- **Uniquely uses resonator structure as optical via for connecting different optical interconnect layers**

Optical Integrated Circuit Optical Via Connections

Optical Integrated Circuit Interconnection Process (1/3)

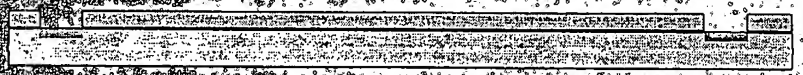
Double sided Optical Interconnect Circuit

1. Grow sacrificial oxide layer

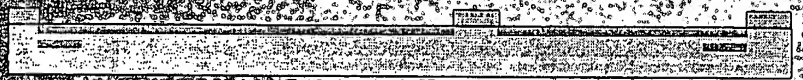


Substrate (Si, GaAs, Sapphire, GaN, etc)

2. Mask and create dopant region for optical via (ex: ion implantation)



3. Creating dopant region for waveguides (ex: ion implantation)



4. Remove mask and continue growth process

5. Creating dopant region for resonator (optical via)

6. Continue growth process and creating dopant region for next level of waveguides

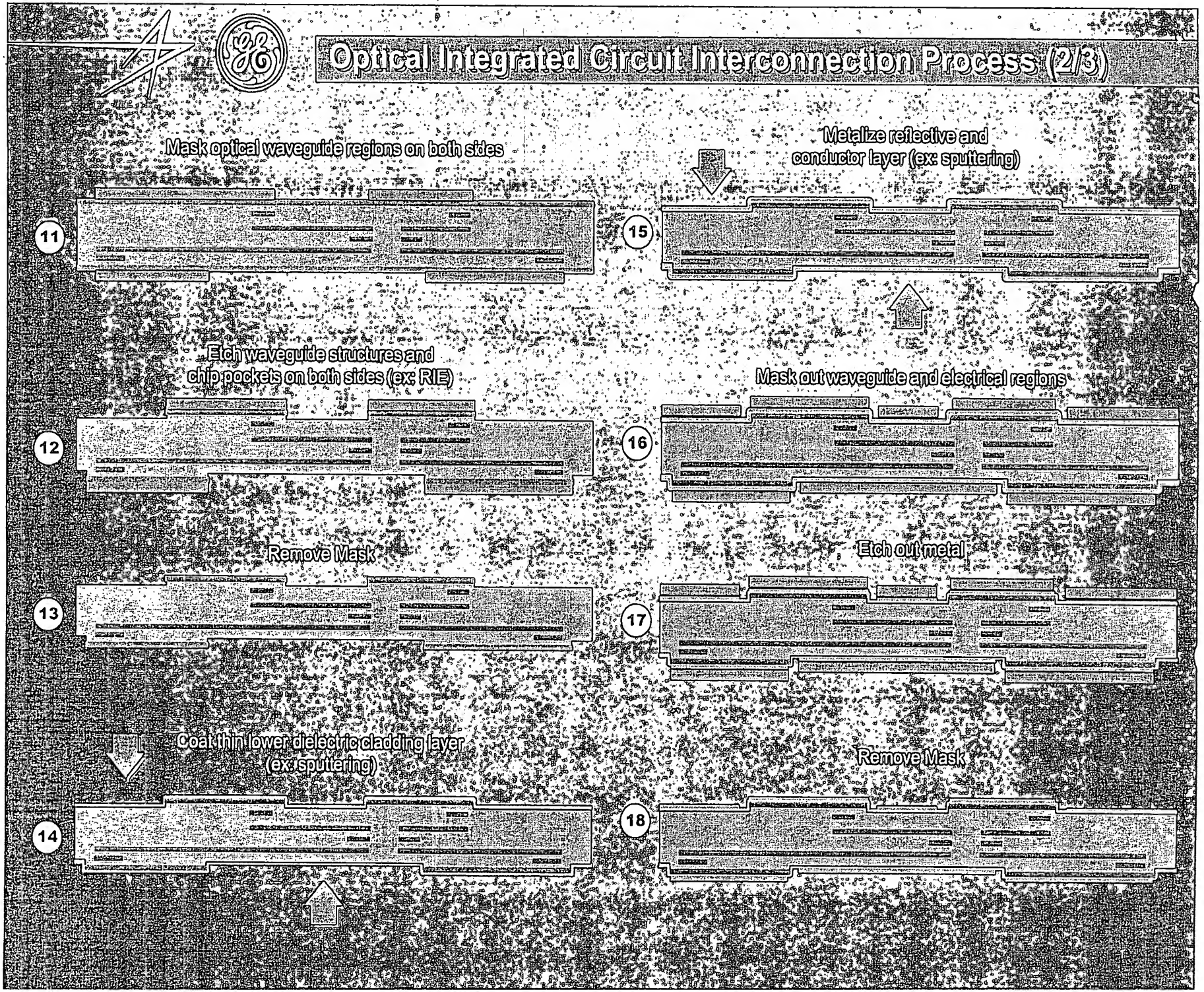
7. Repeat step 2 to 6 for building additional intermediate optical interconnect layers

8. Blanket dope the entire top surface region

9. Etch out sacrificial oxide layer and remove bottom substrate

10. Blanket dope the entire bottom surface region

Optical Integrated Circuit Interconnection Process (2/3)



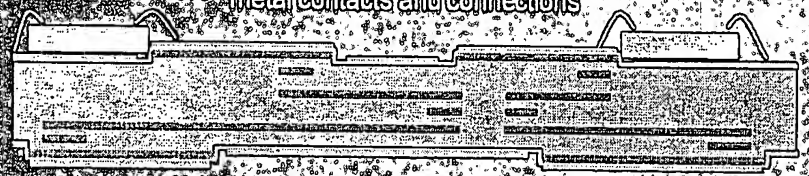
Optical Integrated Circuit Interconnection Process (3/3)

Place optical, electrical and opto-electronic components on top surface

19

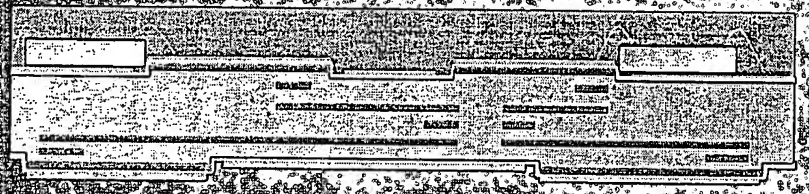
Wire-bond components onto metal contacts and connections

20



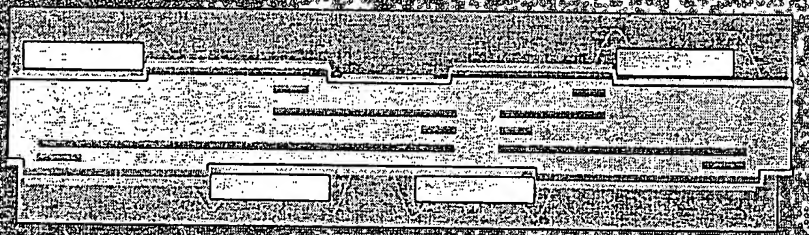
Encapsulate top surface

21



Repeat steps 19-21 for the bottom surface

22



There are two different variations of the concept. The first enables components to be mounted on only one side of the substrate. The Second allows both sides of the substrate to be populated with components.

The single-sided version, using a single substrate, is comprised of the following steps. These steps correspond to the illustrations found in the attachment.

Step 1: The substrate is first masked with the optical waveguide interconnection pattern.
Step 2: A semiconductor-doping technique, such as ion implantation, is used to define the optical waveguides.
Step 3: The mask is removed and regrowth of the substrate material is performed to cover the waveguide.
Step 4: Further masking and doping occurs to construct optical vias (rings, disks, etc.) with a small dielectric gap between the optical vias and the waveguides between layers. The optical via is an optical resonator that couples energy from the waveguide. The coupling efficiency is controlled by the size of the dielectric filled gap between the waveguide and via. Conversely, the optical via can couple energy to a waveguide.
Step 5: The mask is removed and another round of masking and doping follows to produce the next level of waveguides.
Step 6: The steps of growth, masking, doping, mask removal and regrowth are repeated until the desired number of layers of optical interconnects have been reached. By appropriate placing of the optical via laterally, relative to the optical waveguides, the optical signal can be coupled in the same direction, opposite direction, to the right, or to the left relative to the original waveguide from one layer into another. This is illustrated by the attached figures for "Optical Integrated Circuit Optical Via Connections."
Step 7: The entire top layer is doped.
Step 8: A masking step follows to define the waveguides on this surface. In this case, the masking pattern is used to cover the region where the optical waveguides are defined rather than the openings.
Step 9: With the mask in place, etching occurs to create pockets for active device placement.
Step 10: The mask is removed.
Step 11: A thin cladding layer is deposited across the surface, via sputtering or similar technique.
Step 12: An electrically conductive and optically reflective metal is deposited on top of the cladding as an electrical connection layer for the active devices.
Step 13: A masking layer defining the electrical interconnections is placed.
Step 14: Unwanted metal is etched from the exposed regions. Optionally, metal could be left on the waveguides to capture scattered light escaped from the waveguide's cladding and direct it back into the waveguide core.
Step 15: The mask is then removed.
Step 16: Optical, electronic and opto-electronic components are placed on the top surface where the pockets were previously etched out from Step 9.
Step 17: Wirebond connections are made to the metal interconnections on the surface.

Step 18: An optional encapsulant is placed over the top.

The double-sided version, using a single substrate, is comprised of the following steps. These steps correspond to the illustrations found in the attachment.

Step 1: A sacrificial oxide layer is grown on top of the substrate. The oxide will be etched away, removing the substrate in subsequent processsing steps later on.
Step 2: Further regular growth (substrate material) is performed over the oxide. A mask is used to define first level of interconnect. Unmasked regions of the surface are doped using a common technique such as ion implantation. This first layer consists of optical vias, such as ring resonators, etc., to couple light vertically through the structure.
Step 3: After the mask has been removed, growth of the substrate material occurs, followed by masking and then doping. This doped layer is the first optical waveguide layer, which is defined by the mask.
Step 4: The mask is removed and substrate material is grown over the waveguides.
Step 5: Masking and doping create optical vias to connect to the next layer.
Step 6: As before, the mask is removed and growth is performed. Masking and doping follow to create the next waveguide layer. This mask is removed and substrate material growth is repeated.
Step 7: The steps of growth, masking, doping, mask removal and growth (Steps 2 through 6) are repeated until the desired number of layers is achieved. The last layer should contain optical vias in order to connect to the top surface.
Step 8: At the top level, the entire surface is doped.
Step 9: The oxide at the bottom of the structure is then etched away, removing the substrate from the rest of the structure.
Step 10: The newly exposed bottom is then blanket doped.
Step 11: Waveguide regions are then masked off on both sides of the structure.
Step 12: Etching is performed to create the waveguides as well as chip pockets for the active devices.
Step 13: The masks are removed from both sides of the structure.
Step 14: A low-index cladding layer is deposited on both sides for the optical waveguides, via sputtering or other deposition technique.
Step 15: A metal layer for interconnection is then deposited over the cladding material on both sides of the structure.
Step 16: Masks are used to define contact regions and the waveguide regions. If a cladding layer is not used, the metal can be left on the waveguides to capture scattered light.
Step 17: Etching is used to remove unwanted metal from each surface.
Step 18: The masks are removed from both sides of the structure.
Step 19: Optical, electrical and opto-electronic devices are placed on the top surface.
Step 20: Wirebonds are then made between the components and the metal interconnections on the surface.
Step 21: The top surface is then encapsulated.
Step 22: Steps 19 through 21 are repeated for the bottom side of the structure.